REMARKS

Drawings

The Examiner required new formal drawings. Applicants provided new formal drawings herewith.

Claim Rejections – 35 USC § 103(a)

The Examiner rejected Claim 1. Claim 1, in its original form, recites:

1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

lowering said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

annealing said p-type layer at a temperature below 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

The Examiner states:

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bour et al. (US 5,926,726) in view of Koike et al. (US 5,811,319).

Bour et al. teaches a carrier gas of H_2 is introduced with reaction gases NH_3 and TMGa and impurity gas Cp_2Mg to a reactor to form a p-type GaN layer at a temperature of 900°C (col 6, 20-26). After formation of the p-type nitride layer the reactant gases are switched out of the reactor and a gas which prevents the decomposition of the III-V layer at such high growth temperatures, NH_3 is added (col 5, ln 60-65 and col 6, ln 31-35). Bour et al also teaches a reactor is cooled down to a temperature where surface decomposition of as-grown p-type GaN layer will not further occur, where upon attainment of the this temperature, the preventer gas, NH_3, is switched out of the reactor and the remaining cool down occurs in molecular N and acceptor activation is preformed either as the reactor is further cooled or maintained at a temperature of 600°C for 20-40 minutes and during the cool down of the reactor a flow of molecular N, N_2, is maintained in the reactor. (col 6, ln 40-65). Bour et al also teaches the anneal process is a quasi-in-situ anneal, where the reactor is brought to room temperature prior to annealing (col 2, ln 32-45) and that ex-situ post-growth anneals have become a common procedure for laser diode processing (col 2, ln 60-64). Bour et al also teaches acceptor activation is the process of atomic H weakly bonded to Mg or Zn dopant atoms are broken by thermal annealing over a period of time (col 6, 7-15). Bour et al also

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teaches a device which comprises a sapphire substrate upon which is grown a n-type GaN, doped with Si followed by the growth of an active region and is followed by a p-type GaN layer doped with Mg followed by the growth of a cap layer comprising n-type GaN doped with Si (col 8, ln 46-55). Bour et al also teaches that after growth is complete and the reactor cooldown has been accomplished, the n-type cap layer may be removed by etching and the device processed into an operable laser, this reads on applicant's limitation of forming a light emitting diode.

Bour et al does not teach the causing of the acceptor doped layer to a p-type layer have a conductivity and a hole density between 3 x 10^{15} cm^{-3} after said cool down process.

In a method of growing p-type gallium nitride, Koike et al. teaches three p-layers of Mg-doped $Al_{x1}Ga_{1-x}N$ forms a p-layer (61) which acts as a clad layer having a hole concentrations of 5 x $10^{17}/cm^3$, 5 x $10^{17}/cm^3$ and 2 x $10^{17}/cm^3$ and an Mg concentrations of 1 x $10^{20}/cm^3$, 1 x $10^{20}/cm^3$ and 2 x $10^{20}/cm^3$, respectively (col 3, 50-65). Koike also teaches electron rays were uniformly irradiated into the p-layer using a reflective electron beam, where this irradiation changed the p-layer into a p-type conductive semiconductor with a hole concentration of 5 x $10^{17}/cm^3$, 5 x $10^{17}/cm^3$ and 2 x $10^{17}/cm^3$ and a resistivity of 0.5 ohm-cm, 0.8 ohm-cm and 1.5 ohm-cm, respectively (col 5, ln 14-26). Koike et al also teaches forming metal electrode, such as nickel or aluminum, are formed on semiconductor devices utilizing GaN group compounds such as AlGaInN after the semiconductor surface is cleaned by wet chemical etching, utilizing a wet chemical etchant such as buffered hydrogen fluoride (col 1, ln 15-30).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bour with Koike's electron beam irradiation because it would have produced p-type conductive semiconductors with low resistivities.

Applicants respectfully point out that the Summary of the present invention states: "One embodiment of the present invention improves on the conventional process by removing all sources of free hydrogen (typically NH_3) in the epitaxial growth chamber during the post growth cool-down process." (p. 4, l. 1) In contrast, Bour describes: "Then, immediately after the growth of p-type GaN layer 22, a preventor gas is maintained in reactor 10 that provides for atomic N that prevents N outdiffusion ... In the case here, the flow of N precursor, NH_3, is continued in the reactor, as depicted in FIG. 2." (col. 6, ll. 30-35) And: "Thus, the temperature of NH_3 switchout is important. If the sample is permitted to cool down too much before the NH_3 is switched out, ..." (col. 7, ll. 5-6). Clearly, Bour keeps NH_3 flowing in the reactor during the initial part of the cool-down process, just as the "conventional process," described in Applicants' Summary. Bour does this because he is concerned with the outdiffusion of N from the GaN layer, and provides NH_3 to prevent this outdiffusion. In contrast, Applicants eliminate all sources of hydrogen during the **entire** cool-down process, and prevent N outdiffusion by other methods. To reflect this difference more clearly, Applicants amended Claim 1 to recite:

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1. A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

lowering said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially throughout the entire cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

annealing said p-type layer at a temperature below 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

As described above, Bour does not disclose the newly included limitation. Furthermore, Koike does not describe the management of hydrogen in the reaction chamber either. Finally, there is no explicit motivation in either Bour or Koike to combine their methods. Therefore, the amended Claim 1 is not obvious over Bour and Koike alone, or in combination.

The Examiner rejected Claim 2. As the content of Claim 2 was related to the newly included limitation of Claim 1, Claim 2 is cancelled.

The Examiner rejected Claims 3-12 and 14-30 over Bour and Koike, in combination with Takatani, Peng and Nitta. Since Claims 3-12 and 14-30 depend from the independent Claim 1, which has been shown to be allowable, Claims 3-12, and 14-30 are allowable as well.

The Examiner rejected Claim 13. Claim 13 recites:

13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

The Examiner states:

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bour et al. (US 5,926,726) in view of Koike et al. (US 5,811,319).

Referring to claim 13, electron rays were uniformly irradiated into the p-layer using a reflective electron beam, this reads on applicant's limitation of exposing said surface to electromagnetic radiation.

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Claim 13 is also rejected under 35 U.S.C. 103(a) as being unpatentable over Bour et al. (US 5,926,726) in view of Koike et al. (US 5,811,310) as applied to claim 5 above, and further in view of Peng et al. (US 5,895,223).

The combination of Bour et al and Koike et al teach all of the limitations of claim 13, except [sic] exposing said surface to electromagnetic radiation.

In a method of etching nitride, Peng et al teaches dipping a nitride chip in an electrolysis liquid and emitting a UV light with a wavelength of 254 nm to illuminate the nitride chip (col 3, ln 40-46), this reads on applicant's limitation of exposing to electromagnetic radiation, where the electrolysis liquid can be one of KOH as the nitride chip is GaN. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Bour et al, Koike et al and Takatani with Peng's because the UV light would illuminate the nitride chip.

Applicants respectfully point out that an "electron beam," such as the one applied by Bour consists of electrons, whereas an "electromagnetic radiation," such as the one applied by the present invention consists of photons. As such, they are completely different forms of matter. Therefore, Bour does not describe this limitation of the present invention.

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CONCLUSION

For these reasons, it is submitted that all pending Claims, as amended, are in condition for allowance and allowance thereof is requested. If the Examiner's next action is anything other than allowance of all pending Claims, the Examiner is respectfully requested to call Applicants' representative at 415-217-6222.

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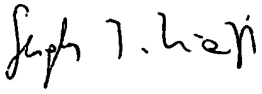
Respectfully submitted,



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ATTACHMENT

Hereby the marked up version of the full claim set is provided, showing all amendments explicitly, in accordance with 37 C.F.R. §1.21(c)(1)(ii). Claims that have not been amended are shown in italics.

1.(Amended) A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

lowering said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially throughout the entire cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

annealing said p-type layer at a temperature below 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

2.(Cancelled) The method of Claim 1 wherein said causing said acceptor-doped layer to be a p-type layer prior to annealing comprises substantially preventing additional hydrogen from diffusing into said acceptor-doped layer during said cooling process.

3.(Amended) The method of Claim [2]1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing

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gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

4.(Amended) The method of Claim [2]1 wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

5. The method of Claim 1 wherein said causing said acceptor-doped layer to be a p-type layer prior to said annealing comprises treating a surface of said acceptor-doped layer to increase said hole density at said surface to be greater than $3x10^{15}cm^{-3}$.

6. The method of Claim 5 wherein said treating said surface comprises chemically etching said surface.

7. The method of Claim 5 wherein said treating said surface comprises plasma etching said surface.

8. The method of Claim 5 wherein said treating said surface comprises plasma cleaning said surface.

9. The method of Claim 5 wherein said treating said surface comprises chemically cleaning said surface.

10. The method of Claim 9 wherein said chemically cleaning said surface comprises cleaning said surface in a solution of at least one of KOH, NaOH, and NH_4OH.

11. The method of Claim 5 wherein said treating said surface comprises ultrasonically cleaning said surface.

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12. The method of Claim 5 wherein said treating said surface comprises irradiating said surface with an electron-beam.

13. The method of Claim 5 wherein said treating said surface comprises exposing said surface to electromagnetic radiation.

14. The method of Claim 1 wherein said growing an acceptor-doped layer results in acceptor impurities in said acceptor-doped layer having greater than 90% passivation prior to said cool-down process.

15. The method of Claim 1 wherein, after said cool-down process, said hole density is greater than $3x10^{16}cm^{-3}$.

16. The method of Claim 1 wherein said introducing acceptor impurities comprises doping said semiconductor layer to have a density of acceptor impurities greater than $5x10^{18}cm^{-3}$.

17. The method of Claim 1 wherein said annealing is carried out at a temperature in the range of 100-625°C.

18. The method of Claim 1 wherein said annealing is carried out at a temperature below 400°C.

19. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer is performed in a chamber different from a chamber in which said p-type layer is annealed.

20. The method of Claim 1 wherein said annealing is carried out after said cool-down process prior to any further processing of said p-type layer.

21. The method of Claim 1 wherein said growing in a chamber an acceptor-doped layer further comprises growing a III-V nitride compound n-doped semiconductor layer to form a light emitting diode.

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22. The method of Claim 21 wherein said acceptor-doped layer is grown subsequent to said n-doped semiconductor layer.

23. The method of Claim 1 further comprising growing additional one or more III-V nitride compound acceptor-doped layers and causing said additional one or more acceptor-doped layers to be p-type prior to said annealing.

24. The method of Claim 1 wherein said annealing is carried out solely to remove said hydrogen from said p-type layer.

25. The method of Claim 1 wherein said annealing is carried out to remove said hydrogen from said p-type layer as well as to anneal or alloy a p-type ohmic contact.

26. The method of Claim 1 wherein said growing said acceptor-doped layer comprises growing a group III-V compound semiconductor including gallium and nitrogen.

27. The method of Claim 1 wherein said acceptor impurities comprise magnesium.

28. The method of Claim 1 wherein said annealing is carried out in a gas environment containing N_2.

29. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 5000 ohm-cm.

30. The method of Claim 1 wherein the resistivity of said p-type layer prior to said annealing is less than 30 ohm-cm.

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